wherein the additional wiring layer, the upper wiring layer and the protective insulation layer are all disposed above the semiconductor substrate; and

wherein the additional wiring layer is formed outside of a region defined by the pad opening section and extending directly under the pad opening section to the semiconductor substrate.

27. (new) A semiconductor device as in claim 26, wherein the second sub-layer upper surface that is contacted by the pad opening section is at an identical vertical level as an upper surface of the insulating layer positioned between the end regions of the first and second sub-layers.

28. (new) A semiconductor device as in claim 27, wherein the first sub-layer includes a lower surface, and the insulating layer positioned between the end regions of the first and second sub-layers includes an additional region having a lower surface positioned at a vertical level that is identical to that of the lower surface of the first sub-layer.

29. (new) A semiconductor device as in claim 26, further comprising a reflection prevention film formed on at least a portion of the upper wiring layer.

30. (new) A semiconductor device as in claim 26, wherein the first and second sub-layers have substantially the same thickness under the pad opening section.

31. (new) A semiconductor device as in claim 30, further comprising a reflection prevention film formed on at least a portion of the upper wiring layer.

32. (new) A semiconductor device as in claim 29, wherein the reflection prevention film is not located on the upper surface of the second sub-layer in the pad opening section.

8 33. (new) A semiconductor device comprising:

a first wiring layer formed above a semiconductor layer and above a first interlayer insulation layer;

a second wiring layer that includes a pad section, the second wiring layer including a first sub-layer and a second sub-layer in direct contact therewith, the second wiring layer formed above the first wiring layer and above a second interlayer insulation layer;

a protective insulation layer formed above the second wiring layer and the second interlayer insulation layer;

a pad opening section exposing part of the second wiring layer, the pad opening section being surrounded by the protective insulation layer; and

a third interlayer insulation layer formed on the second interlayer insulation layer, wherein a portion of the third interlayer insulation layer is positioned between end regions of the first sub-layer and the second sub-layer;

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wherein an upper surface of the first interlayer insulation layer includes a first region where the protective insulation layer is formed vertically thereabove, and the first wiring layer is formed on the first region.

9 34. (new) A semiconductor device as in claim 8 33, wherein the second sub-layer upper surface includes a pad opening section that is contacted by the pad opening section and is at an identical vertical level as an upper surface of the insulating layer positioned between the end regions of the first and second sub-layers.

10 35. (new) A semiconductor device as in claim 9 34, wherein the first sub-layer includes a lower surface, and the third interlayer insulating layer includes a region having a lower surface positioned at a vertical level that is identical to that of the lower surface of the first sub-layer.

11 36. (new) A semiconductor device as in claim 8 33, further comprising a reflection prevention film formed on at least a portion of the upper wiring layer.

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12 37. (new) A semiconductor device as in claim 36, wherein the first and second sub-layers have substantially the same thickness under the pad opening section.

13 38. (new) A semiconductor device as in claim 37, further comprising a reflection prevention film formed on at least a portion of the upper wiring layer.

14 39. (new) A method for manufacturing a semiconductor device, comprising:

forming a lower level wiring layer above a semiconductor substrate;

forming a lower level interlayer insulation layer on and adjacent to the lower level wiring layer;

forming a first sub-layer of an upper level wiring layer above the lower level interlayer insulation layer, wherein the lower level wiring layer is electrically connected to first sub-layer of the upper level wiring layer;

forming an upper level insulation layer on the first sub-layer of the upper level wiring layer;

removing part of the upper level insulation layer so that a portion of the first sub-layer is exposed and end regions of the first sub-layer are covered by the upper level insulation layer;

forming a second sub-layer of the upper level wiring layer on the exposed portion of the first sub-layer and on the upper level insulation layer covering the end regions of the first sub-layer;

forming a protective insulation layer over the second sub-layer and over the upper level insulation layer; and

removing a first portion of the protective insulation layer over a central portion of the second sub-layer to form a pad opening section, wherein a second portion of the protective insulation layer covers an outer portion of the second sub-layer, wherein no portion of the lower level wiring layer is disposed vertically below the pad opening section.

15 40. (new) A method as in claim 14, further comprising forming a reflection prevention film on the second sub-layer prior to forming the protective insulation layer, and, after the removing the first portion of the protective insulation layer, removing the reflection prevention layer so that the reflection prevention film is not present on the second sub-layer in the pad opening section.

16 41. (new) A method as in claim 14, further comprising forming an intermediate level wiring layer and an intermediate level interlayer dielectric layer, wherein the intermediate level wiring layer is positioned above the lower level wiring layer and below the upper level wiring layer, wherein the intermediate level interlayer dielectric layer is positioned above the lower level interlayer dielectric layer and below the upper level wiring layer, and wherein no portion of the intermediate level wiring layer is disposed vertically below the pad opening section.

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17 42. (new) A method as in claim 16, further comprising:

forming the lower level wiring layer to be electrically connected to the intermediate level wiring layer;

forming the intermediate level wiring layer to be electrically connected to the upper level wiring layer;

forming the lower level wiring layer to include a thickness that is less than that of the lower level interlayer dielectric layer;

forming the intermediate level wiring layer to include a thickness that is less than that of the intermediate level interlayer dielectric layer;

forming a plurality of lower level plugs to electrically connect the lower level wiring layer to the intermediate level wiring layer; and

forming a plurality of intermediate level plugs to electrically connect the intermediate level wiring layer to the upper level wiring layer;

wherein the intermediate level plugs are formed to be offset from the lower level plugs in a vertical direction.

18 43. (new) A method as in claim 39, wherein the central portion of the second sub-layer includes an upper surface that is at an identical vertical level as an upper surface of the upper insulating layer that is positioned between end regions of the first and second sub-layers.

19 44. (new) A semiconductor device as in claim 39, wherein the first sub-layer includes a lower surface, and the upper insulating layer includes a region having a lower surface positioned at a vertical level that is identical to that of the lower surface of the first sub-layer.

20 45. (new) A semiconductor device as in claim 39, wherein the first and second sub-layers are formed to have substantially the same thickness under the pad opening section.

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21 46. (new) A method for manufacturing a semiconductor device, the method comprising:

forming a first interlayer insulating layer on a semiconductor substrate;

forming a first wiring layer on the first interlayer insulating layer;

forming a second interlayer insulation layer on the lower wiring layer;

forming a plurality of through-holes in the second interlayer insulating layer that contact the first wiring layer;

forming a second wiring layer on the second interlayer insulation layer and in electrical contact with the first wiring layer through the through-holes;

forming a third interlayer insulating layer on the second wiring layer;

forming a plurality of through-holes in the third interlayer insulating layer that contact the second wiring layer;

forming a first sub-layer of a third wiring layer on the third interlayer insulation layer and in electrical contact with the second wiring layer through the through-holes in the third interlayer insulating layer;

forming an additional insulating layer on the first sub-layer of the third wiring layer;

removing a central portion of the additional insulating layer to expose a region of the first sub-layer of the third wiring layer, wherein an outer portion of the additional insulating layer is not removed;

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forming a second sub-layer of the third wiring layer in direct contact with the exposed region of the first sub-layer, wherein a portion of the second sub-layer is formed above an upper surface of the outer portion of the additional insulating layer;

forming a protective insulation layer on the second sub-layer and on an upper surface of the outer portion of the additional insulating layer; and

forming a pad opening section in the protective insulation layer that reaches the second sub-layer, so that the protective insulating layer extends around the pad opening section.

22 ~~47~~. (new) A method as in claim ~~46~~ 21, further comprising forming the device so that the first and second wiring layers are positioned outside of a region extending vertically below the pad opening section to the semiconductor substrate, and the plurality of through-holes in the third interlayer insulating layer are offset in a vertical direction from the plurality of through-holes in the second interlayer insulating layer.

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23 ~~48~~. (new) A method as in claim ~~46~~ 21, further comprising forming the pad opening section and the first and second wiring layers, and the through-holes so that the first and second wiring layers are positioned outside a region of the pad opening section as viewed in a plan view.

24 ~~49~~. (new) A semiconductor device comprising:

a semiconductor layer;

a first wiring layer formed above the semiconductor layer;

a second wiring layer above the first wiring layer;

a third wiring layer above the second wiring layer;

a protective insulation layer formed above the third wiring layer;

a pad opening section provided in the protective insulation layer;

a plurality of first plugs positioned between the first wiring layer and the second wiring layer;

a plurality of second plugs positioned between the second wiring layer and the third wiring layer;

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wherein the first wiring layer and the second wiring layer are positioned outside a region of the pad opening section as viewed in a plan view;

wherein the plurality of first plugs are positioned in a staggered manner;

wherein the plurality of second plugs are formed in a staggered manner; and

wherein the plurality of first plugs and the plurality of second plugs are positioned to be offset from each other in a vertical direction.

25 ~~50~~. (new) A semiconductor device as in claim ~~49~~ 24;

wherein the plurality of first plugs comprises first, second, third and fourth rows of first plugs, wherein second and fourth rows of first plugs are staggered from the first and third rows of first plugs; and

wherein the plurality of second plugs comprises at least first, second third and fourth rows of second plugs, wherein the second and fourth rows of second plugs are offset from the first and third rows of second plugs.

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26 ~~51~~. (new) A method for manufacturing a semiconductor device, comprising:

forming a first wiring layer above a semiconductor layer;

forming a plurality of first plugs on the first wiring layer;

forming a second wiring layer above the first wiring layer, wherein the plurality of first plugs are disposed between the first wiring layer and the second wiring layer;

forming a plurality of second plugs on the second wiring layer;

forming a third wiring layer above the second wiring layer, wherein the plurality of second plugs are disposed between the second wiring layer and the third wiring layer;

forming a protective insulation layer above the third wiring layer;

forming a pad opening section in the protective insulation layer, which reaches the third wiring layer;

wherein the first wiring layer and the second wiring layer are formed outside a region of the pad opening section as viewed in a plan view,

wherein the plurality of first plugs are formed in a staggered manner;

wherein the plurality of second plugs are formed in a staggered manner; and

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wherein the plurality of first plugs and the plurality of second plugs are positioned to be offset from each other in a vertical direction.

27 52. (new) A method as in claim 26;

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wherein the forming a first plurality of plugs comprises forming first through fourth rows of first plugs so that the second and fourth rows of first plugs are offset from the first and third rows of first plugs; and

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wherein the forming a second plurality of plugs comprises forming first through fourth rows of second plugs so that the second and fourth rows of second plugs are offset from the first and third rows of second plugs.

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